AF 12/26/03

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application No.: 09/483,101
Filed: January 14, 2000
Inventor(s): Kevin J. McGrath and Michael T. Clark

Title: Establishing an Operating Mode in a Processor

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Examiner: Li, Aimee J.
Group/Art Unit: 2183
Atty. Dkt. No: 5500-54700

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on the date indicated below.

Lawrence J. Merkel
Printed Name

Signature 11/18/03 Date

REPLY BRIEF TO EXAMINER'S ANSWER

ATTN: BOX AF
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

In response to the Examiner's Answer mailed October 22, 2003, Appellants present this Reply Brief. Appellants respectfully request that this reply brief be entered pursuant to 37 C.F.R. § 1.193(b)(1) and considered by the Board of Patent Appeals and Interferences.

REMARKS

Appellants thank the Examiner for making copies of the Appeal Brief, since apparently only one copy of the Appeal Brief was in the file wrapper. Appellants are in possession of a date-stamped post card from the PTO evidencing receipt by the PTO of the Appeal Brief in triplicate. Appellants respectfully submit that three copies of the Appeal Brief were submitted.

Comments on Address Size

On page 5, first two lines, the Examiner's Answer alleges that the claims do not exactly specify what "address size" refers to, because address size could refer to the size of the address space or the number of bits needed to represent a valid address. Appellants respectfully submit that the term "address size" is well understood in the art to refer to the number of bits in an address. Even further, claim 17 recites "generating addresses of said default address size", which further clarifies the meaning of the "default address size".

Comments Regarding the DPL field in Turley

Appellants discuss in the Appeal Brief why the DPL field has nothing to do with default address size. The Examiner's Answer alleges that "the DPL bit must match to allow access to the segment of memory. If access is not granted to the segment of memory, the segment cannot be accessed to set the address size" (Examiner's Answer, page 7, lines 15-17 in the right-hand box). The Examiner's Answer further alleges that "whether memory access is granted or denied affects the default address size, because if the DPL indicates that the segment of memory cannot be accessed, then the default address size cannot be set (Turley, page 46, paragraph 4 to page 47 paragraph 1 and page 51, DPL)" (Examiner's Answer, page 13, second paragraph, second sentence).

Appellants respectfully submit that there is nothing in the Turley's segment that sets the address size, or any other attribute of the segment. The segment is merely the memory region that is described by the segment descriptor, and may store instructions or data (See, e.g., Turley page 48, "Segment Descriptors" section). **Segment attributes are determined from the segment descriptor, and the DPL field does not control access to the segment descriptor**. The DPL field is IN the segment descriptor, and thus the segment descriptor must be accessed to even determine the value of the DPL field (See Turley, page 50, Figure 2-2). Also, Turley defines the DPL as "This two bit field indicates the level of privilege associated with the *memory space that the descriptor defines*" i.e., the segment (Turley, page 51, fifth paragraph). Accordingly, it is clear that the DPL field does not control access to the segment descriptor, and that the segment descriptor determines the attributes of the segment (and thus there is no access to the

segment itself to determine address size). The portion of Turley referred to in the Examiner's answer (page 46, paragraph 4 to page 47, paragraph 1), does not support the contention that the address size cannot be set if the segment of memory cannot be accessed. Instead, this section states that "A program that tries to traverse the entire 4GB address space of the 80386 merely by incrementing an index repeatedly would probably be greeted by a segment violation exception at some point along the way" (Turley, page 47, lines 3-6). Thus, Turley teaches that addresses are generated, and the generated address causes a segment violation exception. Thus, while the access is not permitted, the size of the address is not limited by the occurrence of the exception.

The Examiner's Answer further alleges "When the DPL does not allow access to the memory segment, a new default address size cannot be set, since information from the segment, specifically the G bit, is required." (Examiner's Answer, page 13, second paragraph, third sentence). As highlighted above, the G bit is in Turley's segment descriptor, not in his segment. The G bit is in the same segment descriptor as the DPL, and thus the DPL does not prevent or deny access to the G bit.

The Examiner's Answer further alleges "if the DPL indicates that certain areas of the memory space defined by the G bit are not accessible (Turley page 46, paragraph 4 to page 47, paragraph 1 and page 51, DPL), the address space size is decreased since those locations are no longer usable by the application" (Examiner's Answer, page 13, second paragraph, fourth sentence). This is NOT what Turley describes on page 46-page 47. There is no teaching that the DPL indicates that certain areas of the memory space defined by the G bit are not accessible. Instead, Turley teaches "a program, no matter how privileged, cannot access an area of memory unless that area has been 'described' to it" (Turley, page 46, last two lines to page 47, line 1). Of course, the mechanism for describing areas of memory is the segment descriptor (see Turley, page 48, "Segment Descriptors" section, first sentence). Thus, the DPL cannot define certain areas defined by the G bit as not accessible. Rather, an entire segment is either accessible or not, dependent on the privilege level and the DPL, not certain portions thereof. Therefore, the DPL is NOT the first operating mode indication, as alleged in the Examiner's Answer.

The Examiner's Answer further alleges that the DPL determines if it is even possible to set a new default address size and whether the space defined is accessible (Examiner's Answer, page 13, last 2 lines to page 14, line 1). While the DPL may determine if the segment is accessible, it has no effect on the default address size since the default address size is determined from the segment descriptor, not the segment itself.

Comments Regarding the "G" Bit in Turley

The Examiner's Answer asserts that "in general, the following equations are used to find what the actual Limit, also know as the maximum address location, is and the address space size (Turley page 50 and page 54).

Actual Limit = Limit Field * G bit measurement

Address Space Size = Actual Limit - Base" (Examiner's Answer, page 10, end of first paragraph).

The second equation (Address Space Size) is incorrect, if one presumes that the address space size is the size of the segment, which Figure 1 (Examiner's Answer, page 12) seems to indicate. Turley teaches that "Intel has defined the limit field as the length of the segment in bytes minus 1" (Turley, page 50, second paragraph). Thus, the size of the segment (the second equation, above) is the actual limit, not the Actual Limit - Base. The segment runs from the base address to the base address + limit. To illustrate the correct relationship between the base address, the limit, and the memory addresses within the segment, Applicants have attached Fig. 3 hereto as Exhibit A. Fig. 3 is numbered as such so as not to conflict with Figures 1 and 2 in the Examiner's Answer. In Fig. 3, the base has been defined as 1,000,000, rather than 0 as in Figure 1. Accordingly, addresses in the segment run from 1,000,000 to 1,000,100 (if G=0) and 1,000,000 to 1,409,600 (if G=1).

The Examiner's Answer goes on to allege that the G bit defines the number of bits in the effective address size (Examiner's Answer, page 11, second paragraph). It is unclear what the "effective address" is in this analysis. However, Applicants disagree

that the G bit defines the number of bits in any address size. The Examiner's Answer states that "The 'X' bits following bit positions 6 and 19 represent bits that, when set to anything other than zero, produce illegal effective addresses" (Examiner's Answer, page 11, second paragraph, page 4). Thus, even the Examiner's Answer effectively admits that addresses may have a larger default address size than would be indicated by the limit, but that some values of the address may be defined by the limit field as being illegal (and thus may cause a segment limit exception). Turley does not teach that illegal addresses cannot be generated, but rather that illegal addresses cause a segment limit violation exception. For example, Turley teaches "If one of your programs erroneously (or deliberately) generates such an invalid address, the processor will trap the offending instruction before attempting to read or write the undefined address" (Turley, page 48, last 2 lines to page 49 first two lines). That is, the address size is not affected by the segment limit, but rather addresses (of the default address size) which violate the segment limit cause an exception.

In fact, in the example given in the Examiner's Answer, even some encodings of bits 6 to 0 (for G=0) and of bits 19 to 0 (for G=1) are "illegal addresses". For example, an encoding of all binary ones in bits 6 to 0 (for G=0) or bits 19 to 0 (for G=1) are "illegal addresses". Accordingly, 6 bits and 19 bits are not the effective address size, according to the analysis in the Examiner's answer, because some encodings of the bits are "illegal".

Comments on Claim Grouping

With regard to the grouping of the claims, Appellants submit that the grouping presented in the Appeal Brief is correct and complies with 37 C.F.R. § 1.192(c)(7). The Examiner's Answer notes that the Appeal Brief, when discussing claim 17, refers to the arguments of claim 1. This is true. However, additional arguments are also presented for claim 17 (see Appeal Brief, page 6, last paragraph continuing on to page 7). Despite the Examiner's assertion (Examiner's Answer, page 15, last paragraph) that page 176, paragraph 1 and page 178, paragraphs 2-3 were cited for further explanation of the art, these sections were cited in the rejection of claim 17 with regard to the highlighted claim features in a different manner than claim 1 (and page 176 was not cited at all with regard

to claim 1). Accordingly, Applicants pointed out why these additional sections did not teach the features of claim 17 as alleged, which is an additional argument of patentability for claim 17.

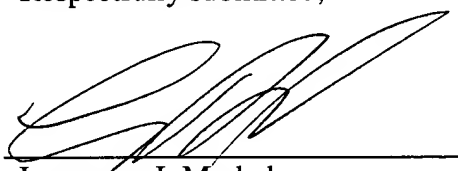
CONCLUSION

For the foregoing reasons and those set forth in the Appeal Brief, it is submitted that the Examiner's rejection of claims 1 and 17 was erroneous, and reversal is respectfully requested.

This Reply Brief is submitted in triplicate along with a return receipt postcard.

If any fees are due, the Commissioner is authorized to charge said fees to Meyertons, Hood, Kivlin, Kowert, & Goetzel, P.C. Deposit Account No. 501505/5500-54700/LJM.

Respectfully submitted,



Lawrence J. Merkel
Reg. No. 41,191
AGENT FOR APPLICANT(S)

Meyertons, Hood, Kivlin, Kowert, & Goetzel, P.C.
P.O. Box 398
Austin, TX 78767-0398
Phone: (512) 853-8800

Date: 11/18/03

When G=0,
Base=1000000,
Limit=100

When G=0,
Base=1000000,
Limit=100

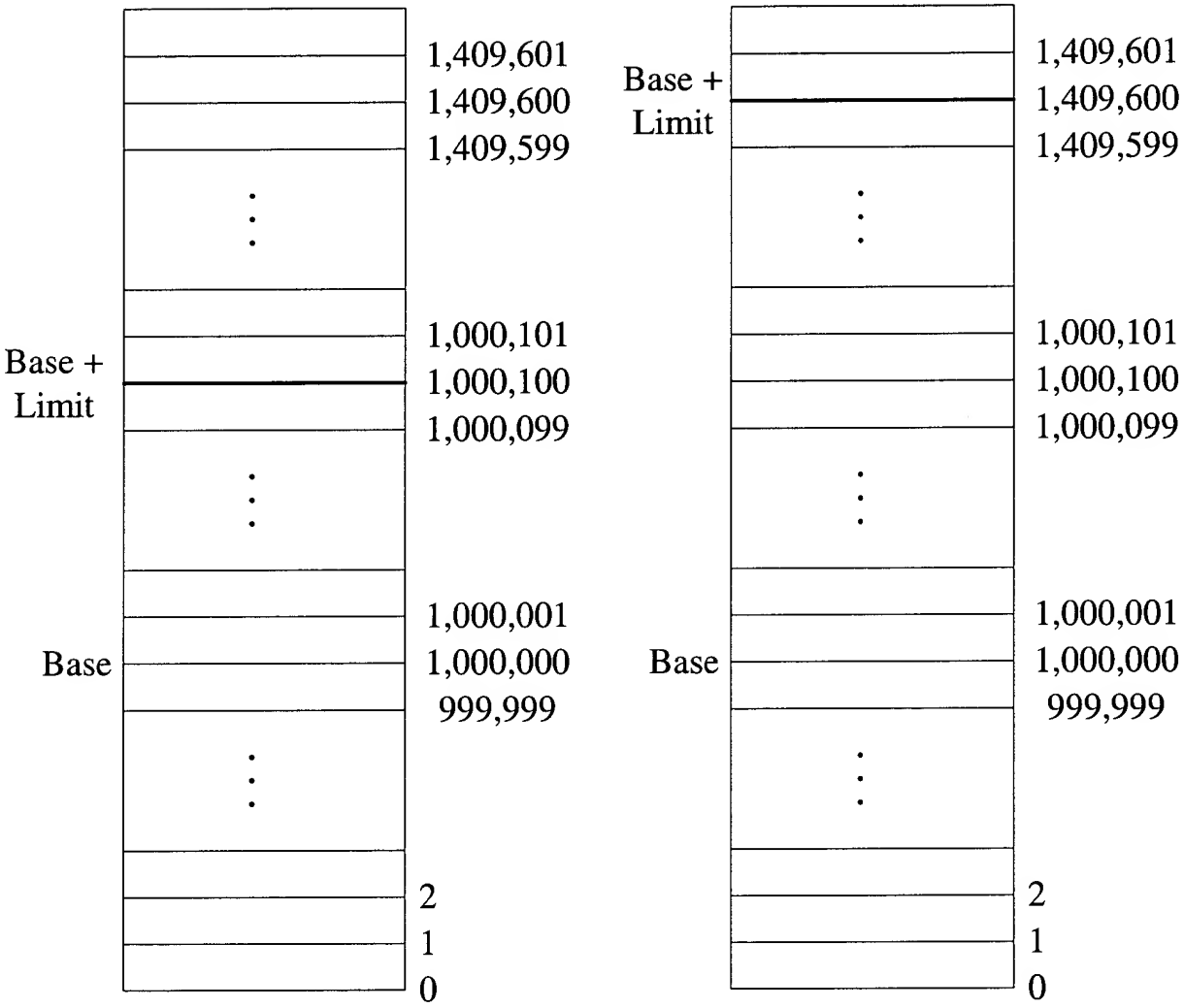


Fig. 3